GAL22V10/883

High Performance E²CMOS PLD Generic Array Logic™

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — 10 ns Maximum Propagation Delay
  - — Fmax = 166 MHz
  - — 7ns Maximum from Clock Input to Data Output
  - — TTL Compatible 12 mA Outputs
  - — UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - — Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices
- **50% REDUCTION IN POWER VERSUS BIPOLAR**
- **E² CELL TECHNOLOGY**
  - — Reconfigurable Logic
  - — Reprogrammable Cells
  - — 100% Tested/100% Yields
  - — High Speed Electrical Erasure (<100ms)
  - — 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
  - — Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - — 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - — DMA Control
  - — State Machine Control
  - — High Speed Graphics Processing
  - — Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

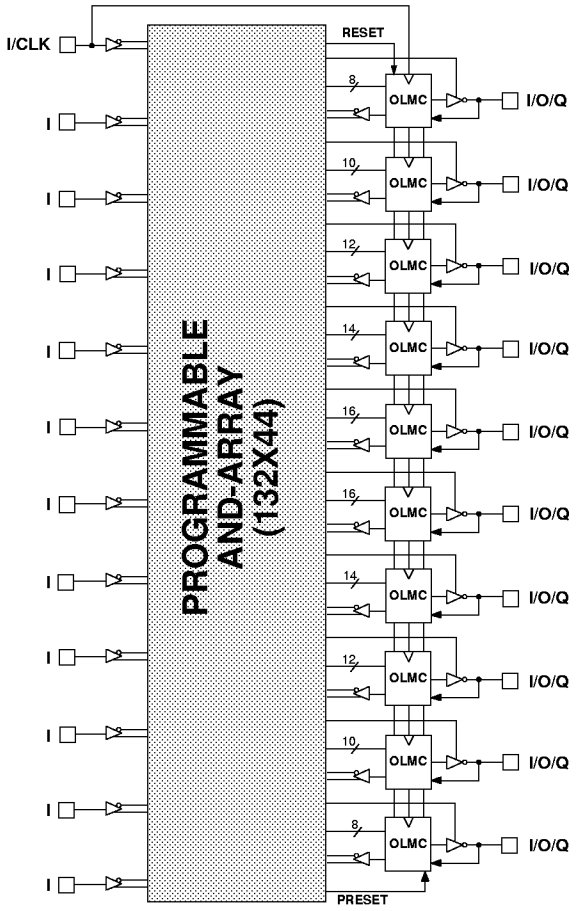
Description

The GAL22V10/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available of any military qualified 22V10 device. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

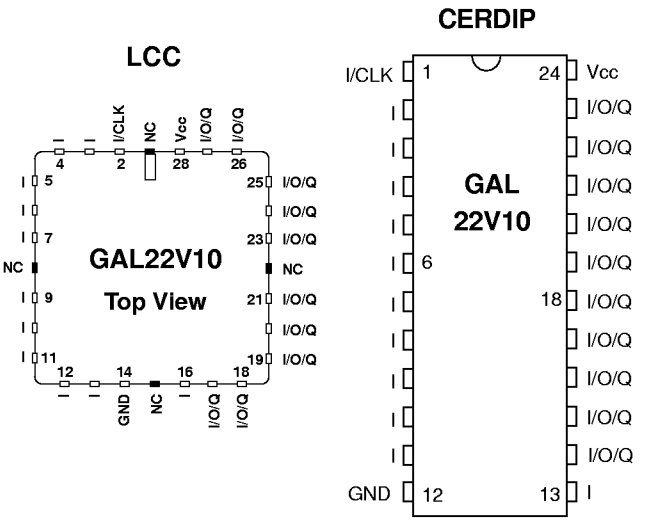
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram



Pin Configuration



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-888-ISP-PLDS; FAX (503) 681-3037; http://www.latticesemi.com

February 1999

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Case Temperature (T_C) ..... -55 to 125°C
Supply Voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss - 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V, f_{toggle} = 15MHz Outputs Open, L -10/-15/-20/-25/-30	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-10		-15		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	—	10	—	15	ns
tco	A	Clock to Output Delay	—	7	—	8	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	8	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	6	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	76.9	—	50	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	76.9	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	166	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	3	—	8	—	ns
twl	—	Clock Pulse Duration, Low	3	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	10	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	12	—	15	ns
tar	A	Input or I/O to Asynchronous Reset of Register	—	12	—	20	ns
tarw	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	6	—	15	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	10	—	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

Capacitance (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	—	20	—	25	—	30	ns
tco	A	Clock to Output Delay	—	15	—	20	—	20	ns
tcf[2]	—	Clock to Feedback Delay	—	15	—	20	—	20	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	17	—	20	—	25	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with No Feedback	33	—	33	—	25	—	MHz
twh	—	Clock Pulse Duration, High	15	—	15	—	20	—	ns
twl	—	Clock Pulse Duration, Low	15	—	15	—	20	—	ns
ten	B	Input or I/O to Output Enabled	—	20	—	25	—	25	ns
tdis	C	Input or I/O to Output Disabled	—	20	—	25	—	25	ns
tar	A	Input or I/O to Asynchronous Reset of Register	—	25	—	30	—	30	ns
tarw	—	Asynchronous Reset Pulse Duration	20	—	25	—	30	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	20	—	25	—	30	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	17	—	20	—	25	—	ns

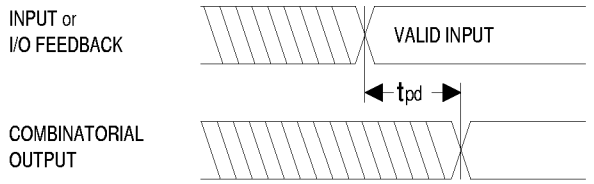
1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

Capacitance (T_A = 25°C, f = 1/0 MHz)

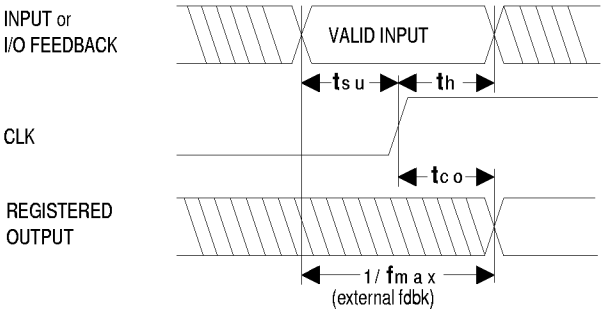
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

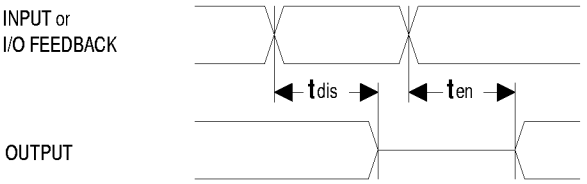
Switching Waveforms



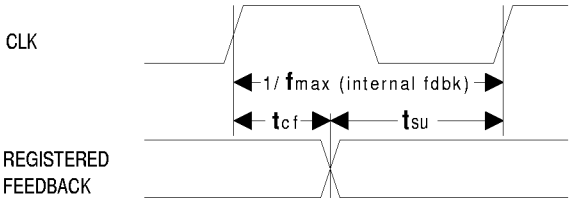
Combinatorial Output



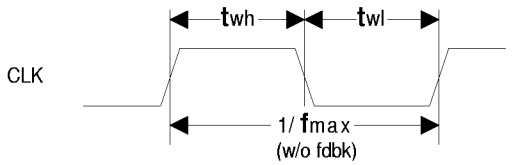
Registered Output



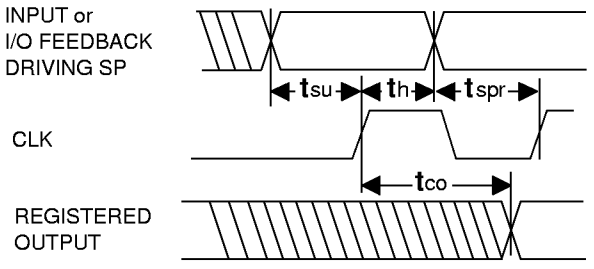
Input or I/O to Output Enable/Disable



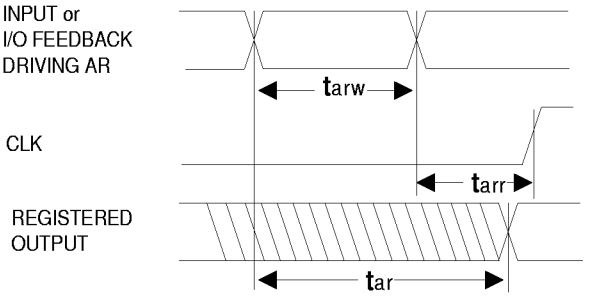
fmax with Feedback



Clock Width

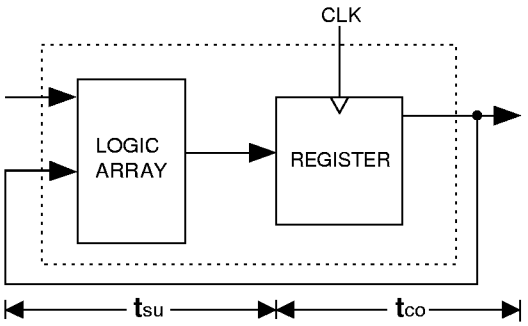


Synchronous Preset



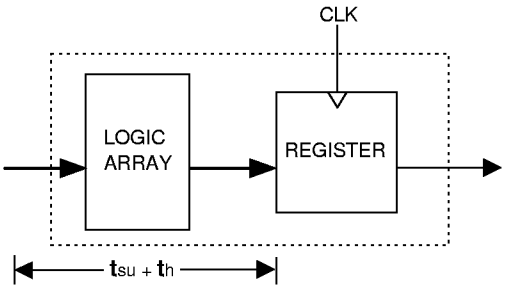
Asynchronous Reset

fmax Descriptions



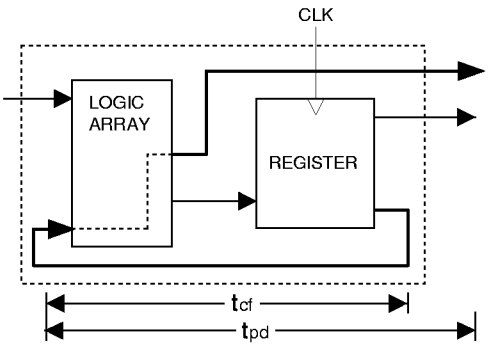
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

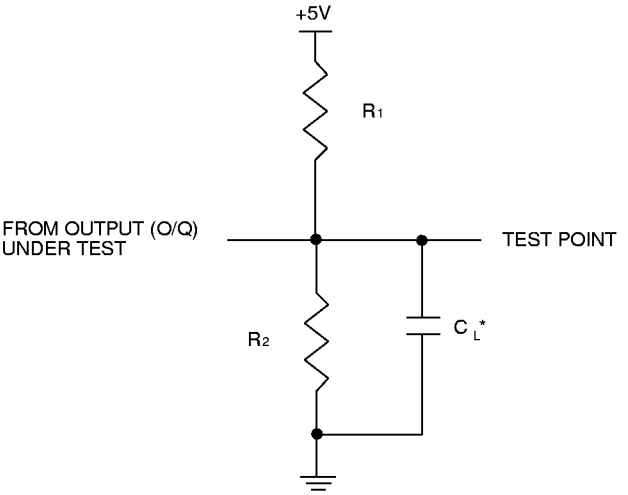
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		390Ω	750Ω	50pF
B	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
C	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL22V10 Ordering Information (MIL-STD-883 and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883**	**SMD #**
10	6	7	150	24-Pin CERDIP	GAL22V10D-10LD/883	5962-8984106LA
			150	28-Pin LCC	GAL22V10D-10LR/883	5962-89841063A
15	12	8	150	24-Pin CERDIP	GAL22V10D-15LD/883	5962-8984103LA
			150	28-Pin LCC	GAL22V10D-15LR/883	5962-89841033A
20	17	15	150	24-Pin CERDIP	GAL22V10D-20LD/883	5962-8984102LA
			150	28-Pin LCC	GAL22V10D-20LR/883	5962-89841023A
25	20	20	150	24-Pin CERDIP	GAL22V10D-25LD/883	5962-8984104LA
30	25	20	150	24-Pin CERDIP	GAL22V10D-30LD/883	5962-8984101LA

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Part Number Description